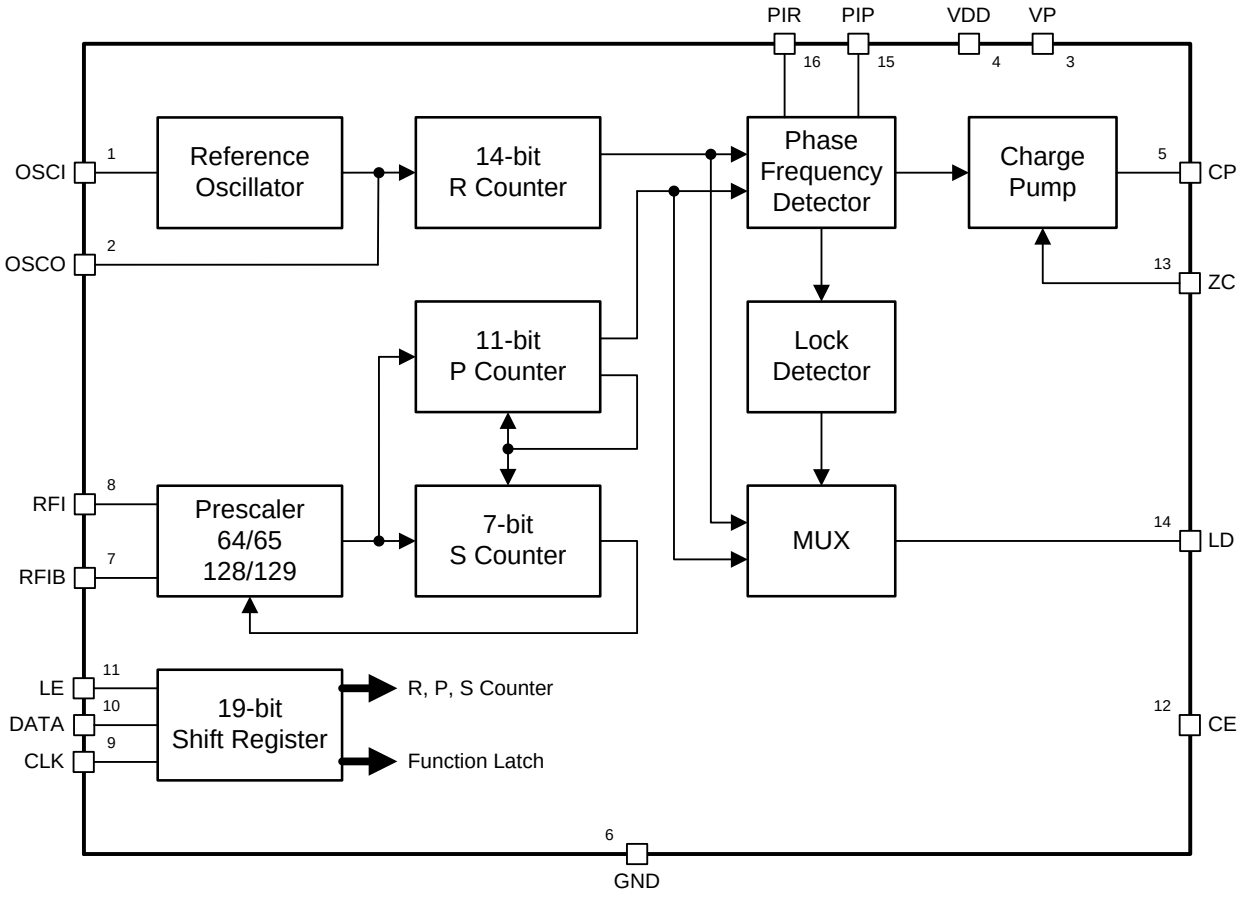
The DHL612 is an integrated frequency synthesizer with prescaler. It consists of a dual-modulus prescaler(64/65, 128/129), programmable P(11-bit) and S(7-bit) counter, programmable R(14-bit) counter, a phase frequency detector(PFD) and a charge pump(1.5mA, 6mA). A PLL can be completely implemented with external loop filter and VCO(voltage controlled oscillator).

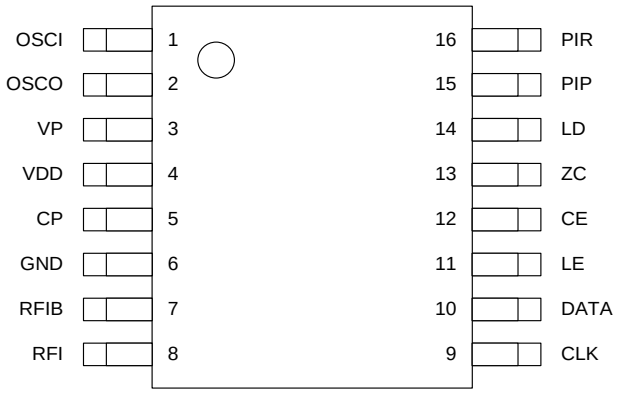
Features

- Maximum 1.2GHz operation
- Low supply current consumption (2.2mA@3V, 2.4mA@5V)
- Wide supply voltage range (2.4V ~ 5.5V)
- 3-wire serial interface
- Power-down mode
- Lock detection
- MB15E03SL compatible

Block Diagram



Pin Description



Pin No.	Mnemonic	I/O	Description
1	OSCI	I	Reference Oscillator input.
2	OSCO	O	Reference Oscillator output.
3	VP	-	Charge pump power supply.
4	VDD	-	Power supply.
5	CP	O	Charge pump output.
6	GND	-	Ground
7	RFIB	I	Complementary RF input. A bypass capacitor should be placed to the ground plane.
8	RFI	I	RF input. This pin should be ac-coupled from the VCO
9	CLK	I	Serial clock input. (Do not open)
10	DATA	I	Serial data input. (Do not open)
11	LE	I	Serial data load enable. (Do not open)
12	CE	I	Chip Enable. (Do not open)
13	ZC	I	The charge pump output(CP) high-impedance control. Internal pull-up resistor.
14	LD	O	Lock detect output(LDS=”L”) or Counter output(LDS=”H”).
15	PIP	O	Phase comparator N-channel open drain output for an external charge pump. NMOS open drain output.
16	PIR	O	Phase comparator CMOS output for an external charge pump.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Power Supply Voltage		V_{DD}	-0.3 to 6.5	V
		V_P	-0.3 to 6.5	V
Input/Output Voltage		V_{IN}, V_{OUT}	-0.3 to V_{DD}+0.3	V
CP Output Voltage		V_{CP}	-0.3 to V_P+0.3	V
Storage Temperature Range		T_{ST}	-55 to +125	°C
ESD	HBM (Human Body Model)	V_{HBM}	2000	V
	MM (Machine Model)	V_{MM}	200	V

This device is a high performance RF integrated circuit and is ESD sensitive. Proper precautions should be taken for handling and assembly.

Recommended Operating Conditions

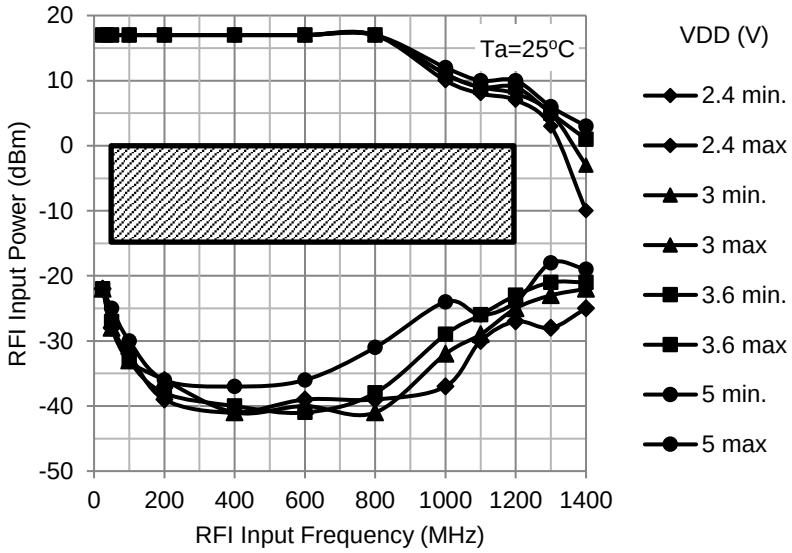
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	2.4 to 5.5	V
	V_P	V_{DD} to 5.5	V
Operating Temperature Range	T_{OP}	-40 to +85	°C

Electrical Characteristics

(V_{DD}=3V, V_P=5V, Ta=-40°C ~ 85°C)

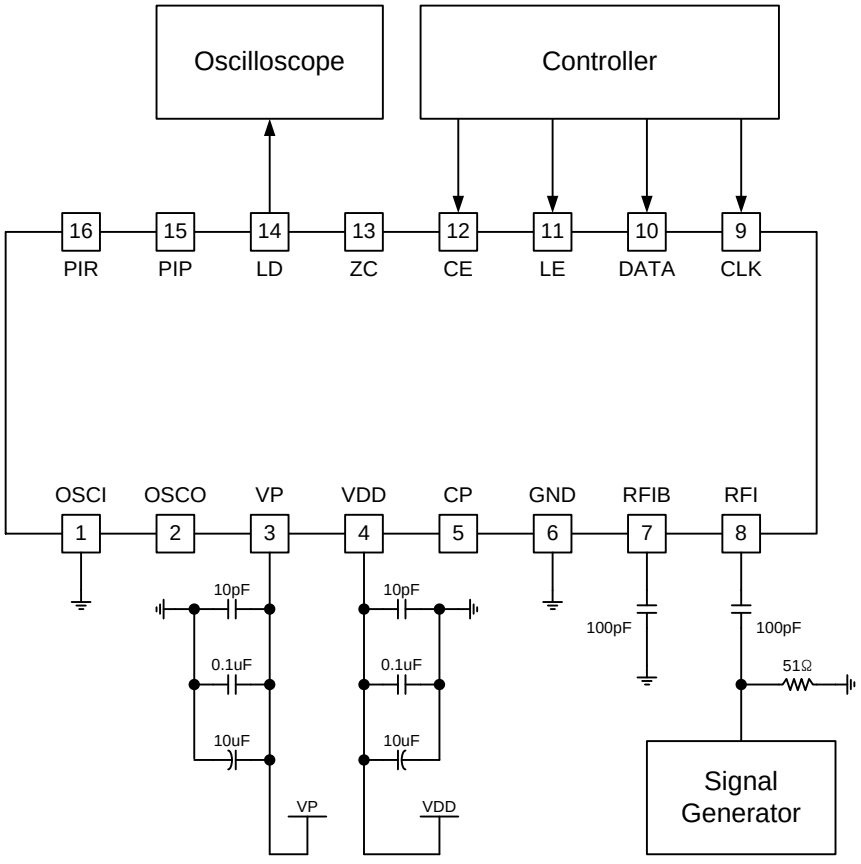
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD}	f_{IN} = 850MHz f_{OSC} = 10MHz In Locking State	V_{DD}=3V		2.2		mA
			V_{DD}=5V		2.4		mA
Power Down Current	I_{CE}	CE=0V			0.1	10	uA
RFI Input Operating Frequency	f_{IN}			50		1200	MHz
OSCI Input Operating Frequency	f_{OSC}			3		40	MHz
RFI Input Sensitivity Power	P_{FIN}			-15		0	dBm
OSCI Input Voltage	V_{OSC}			0.5		3	Vp-p
Logic High-Level Input Voltage	V_{IH}			V_{DD}X0.7			V
Logic Low-Level Input Voltage	V_{IL}					V_{DD}X0.3	V
Logic High-Level Input Current	I_{IH}			0		1	uA
Logic Low-Level Input Current	I_{IL}			-1		0	uA
OSCI High-Level Input Current	I_{IHOSC}			0		100	uA
OSCI Low-Level Input Current	I_{ILOSC}			-100		0	uA
ZC Low-Level Input Current	I_{ILZC}			-100		0	uA
Logic High-Level Output Voltage	V_{OH}	I_{OH} = -1mA		V_{DD}–0.4			V
Logic Low-Level Output Voltage	V_{OL}	I_{OL} = 1mA				0.4	V
CP High-Level Output Current	I_{OHCP}	V_{CPO}=2.5V, CS=High			-6		mA
		V_{CPO}=2.5V, CS=Low			-1.5		mA
CP Low-Level Output Current	I_{OLCP}	V_{CPO}=2.5V, CS=High			6		mA
		V_{CPO}=2.5V, CS=Low			1.5		mA
CP Cutoff Leakage Current	I_{LEAKCP}	V_{CPO}=0.5V to 4.5V			1		nA
CP Output Current Mismatch	I_{OHCP} vs I_{OLCP}	V_{CPO}=2.5V, T_A=25°C				15	%
	vs V_{CPO}	V_{CPO}=0.5V to 4.5V				20	%
	vs Ta	V_{CPO}=2.5V, T_A=- 40 to 85°C			3		%

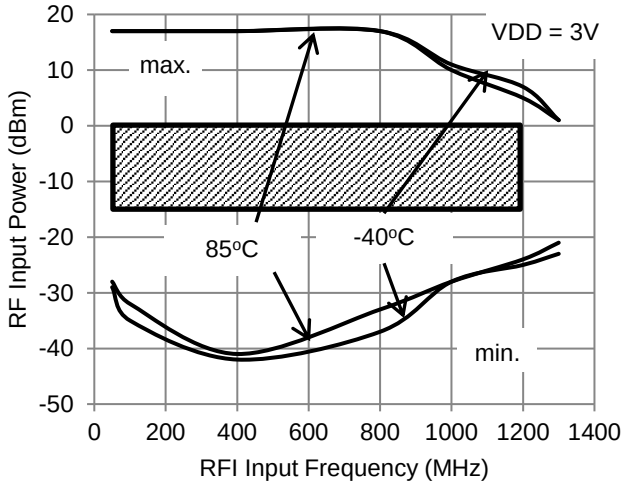
Typical Performance Characteristics

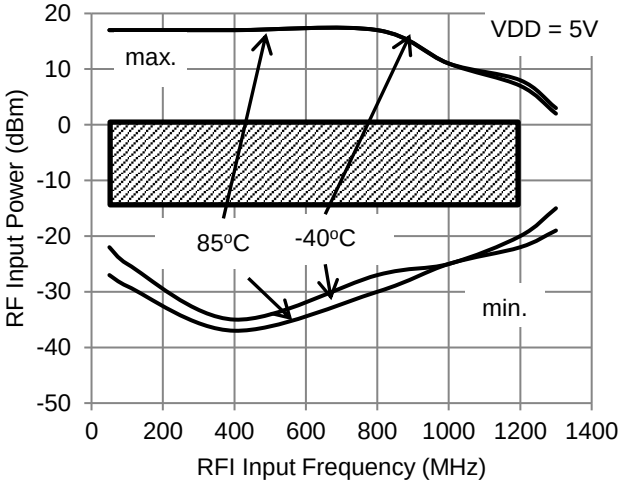


RF Input Sensitivity vs Power Supply Voltage (64/65 mode)

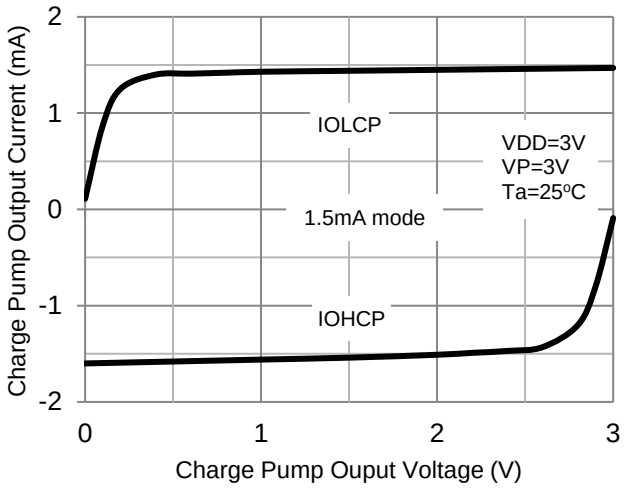
RF Input Sensitivity Measurement Circuit

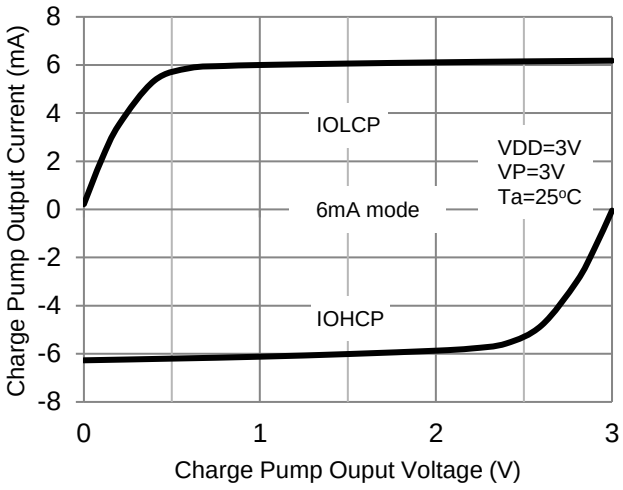


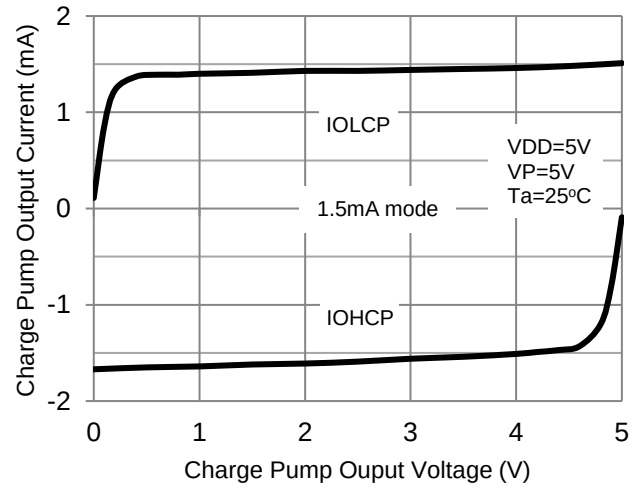


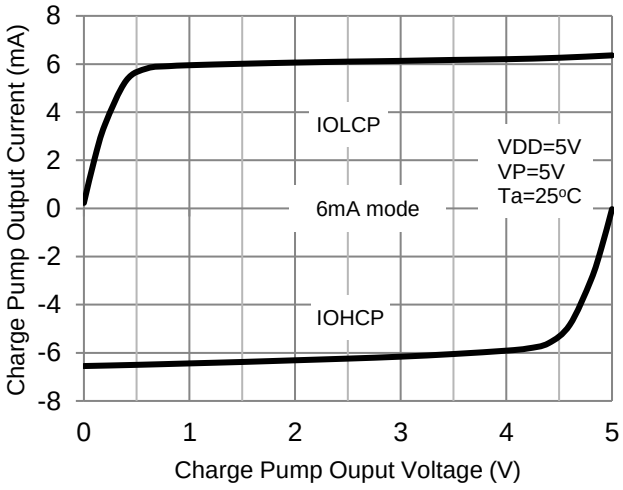


RF Input Sensitivity vs Temperature (64/65 mode)

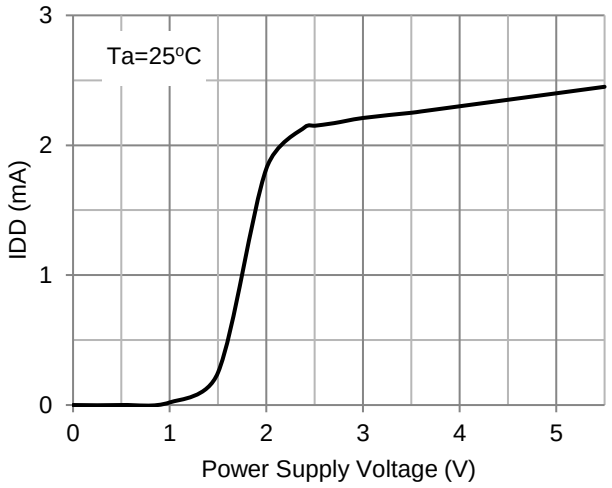






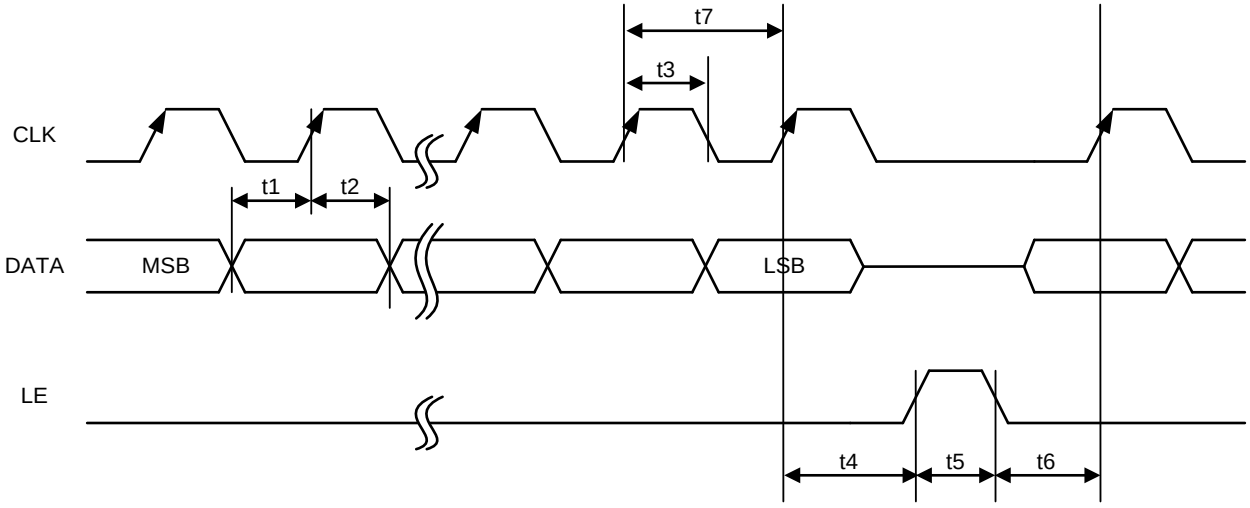


Charge Pump Output Characteristics



Power Supply Current Consumption

Serial Data Input Timing Characteristics



Parameter	Minimum Limit	Unit	Description
t1	20	ns	DATA to CLK setup time
t2	20	ns	DATA to CLK hold time
t3	30	ns	CLK pulse width high
t4	30	ns	CLK to LE setup time
t5	100	ns	LE pulse width high
t6	20	ns	LE to CLK setup time
t7	100	ns	CLK period

Serial Data Input Description

Control Bit

CNT	Destination of Serial Data
H	Reference(R) Counter and Function Latch
L	Program(P) Counter and Swallow(S) Counter Latch

Reference(R) Counter and Function Latch

MSB																		LSB
Function				14-bit Reference Counter														CNT
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
CS	LDS	FC	SW	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	“H”

CNT : Control Bit

Function

CS	Charge Pump Current
H	6mA
L	1.5mA

LDS	LD Pin Selection
H	Divided Signal
L	Lock Detect Signal

FC	PFD Polarity
H	positive
L	negative

SW	Prescaler Divide Ratio
H	64/65
L	128/129

PFD : Phase Frequency Detector

14-bit Reference Counter

Divide Ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•••	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Divide Ratio : 3 to 16383

Divide ratios Less than 3 are prohibited.

LDS	FC	LD Pin Selection
H	H	Divided Signal of Reference Input (OSCI)
	L	Divided Signal of RF Input (RFI)
L	Don’t Care	Lock Detect Signal

Program(P) Counter and Swallow(S) Counter Latch

MSB																		LSB
11-bit Program Counter											7-bit Swallow Counter							CNT
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	S7	S6	S5	S4	S3	S2	S1	“L”

CNT : Control Bit

11-bit Program Counter

Divide Ratio	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•••	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide Ratio : 3 to 2047

Divide ratios Less than 3 are prohibited.

7-bit Swallow Counter

Divide Ratio	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•••	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Divide Ratio : 0 to 127

Pulse Swallow Function

The equation for the VCO frequency is as follows :

$$f_{VCO} = \{(M \times P) + S \} \times f_{REF} / R \ (S < P)$$

For continuously adjacent divide ratio {(M x P) + S} , minimum divide ratio is ($M^2 - M$).

f_{VCO} : The output frequency of external voltage controlled oscillator(VCO)

M : The preset modulus of dual-modulus prescaler (64 or 128)

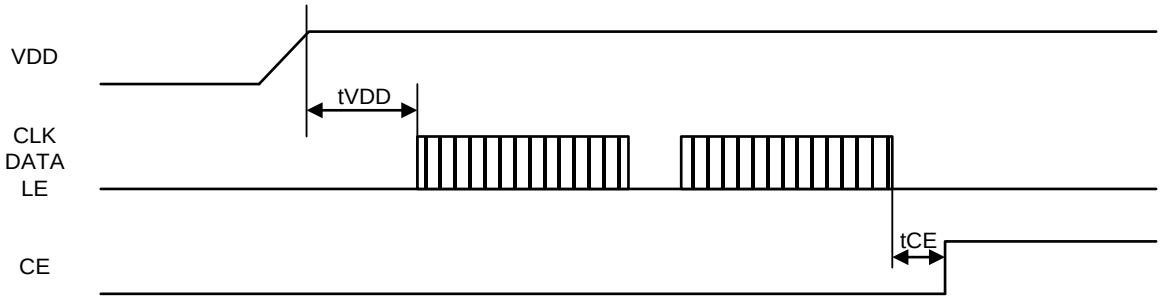
P : The preset divide ratio of binary 11-bit program(P) counter (3 to 2,047)

S : The preset divide ratio of binary 7-bit swallow(S) counter (0 to 127)

f_{REF} : The output frequency of the reference frequency oscillator

R : The preset divide ratio of binary 14-bit reference(R) counter (3 to 16,383)

Programming after Initial Power Up



Parameter	Minimum Limit	Unit	Description
tVDD	1	us	VDD to serial data input sequence setup time
tCE	100	ns	CE to serial data input sequence hold time

Power Down (CE pin)

CE Pin (Input)	Status
H	Normal operation
L	Power Down

The complete power down is controlled by the external pin CE. In the power down state, the power consumption is lowered, the charge pump output becomes high impedance state, but the registers are still operational enabling programming of the device. The power down is immediate and asynchronous.

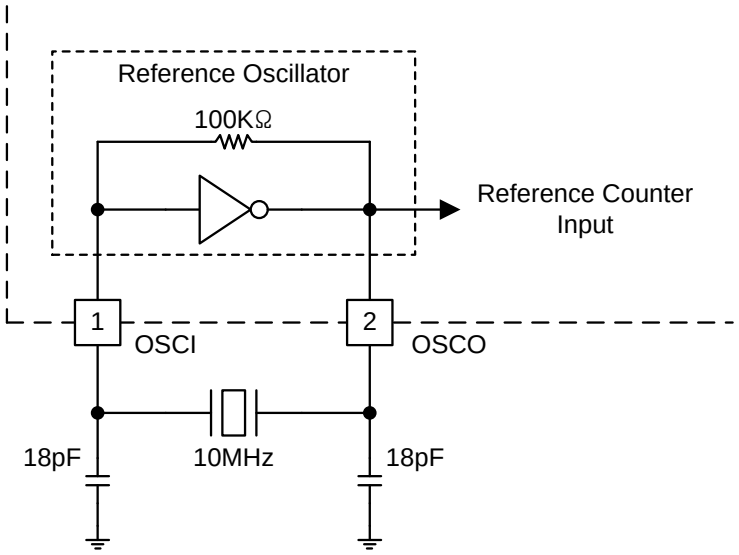
Charge Pump Output Control (ZC pin)

ZC Pin (Input)	Charge Pump
H	Normal operation
L	High impedance output

Lock Detect (LD pin)

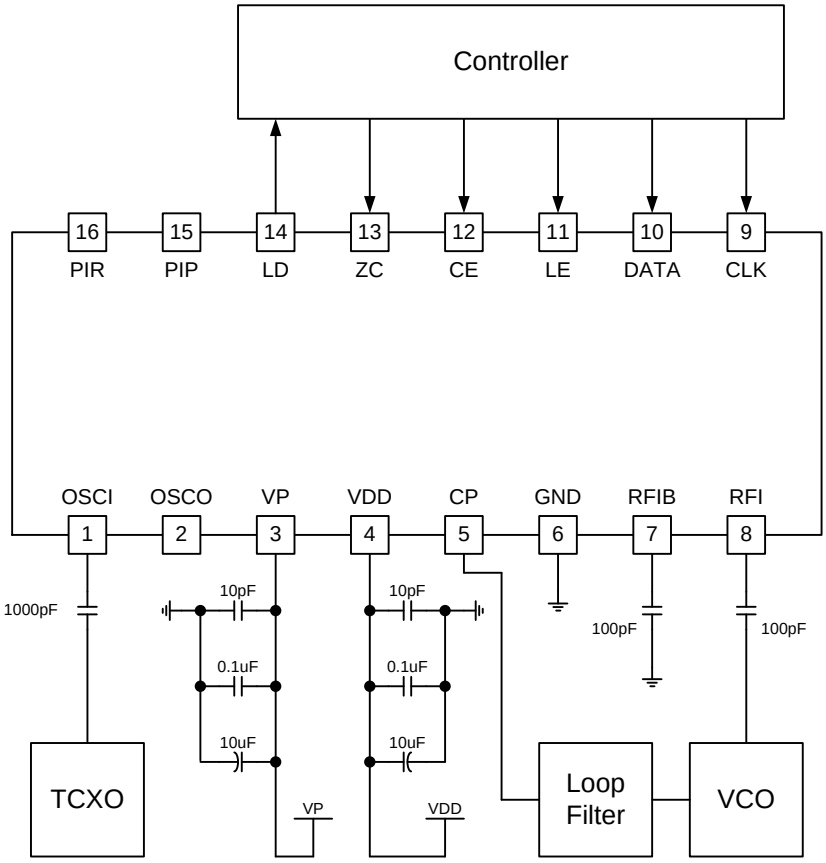
LD Pin (Output)	LDS Latch	Lock State
H	L	Detected
L		NOT Detected

Crystal Oscillator Application using Reference Oscillator



The capacitor values need to be optimized to provide accurate matching between the crystal and the IC.

Application Example



Package Dimensions