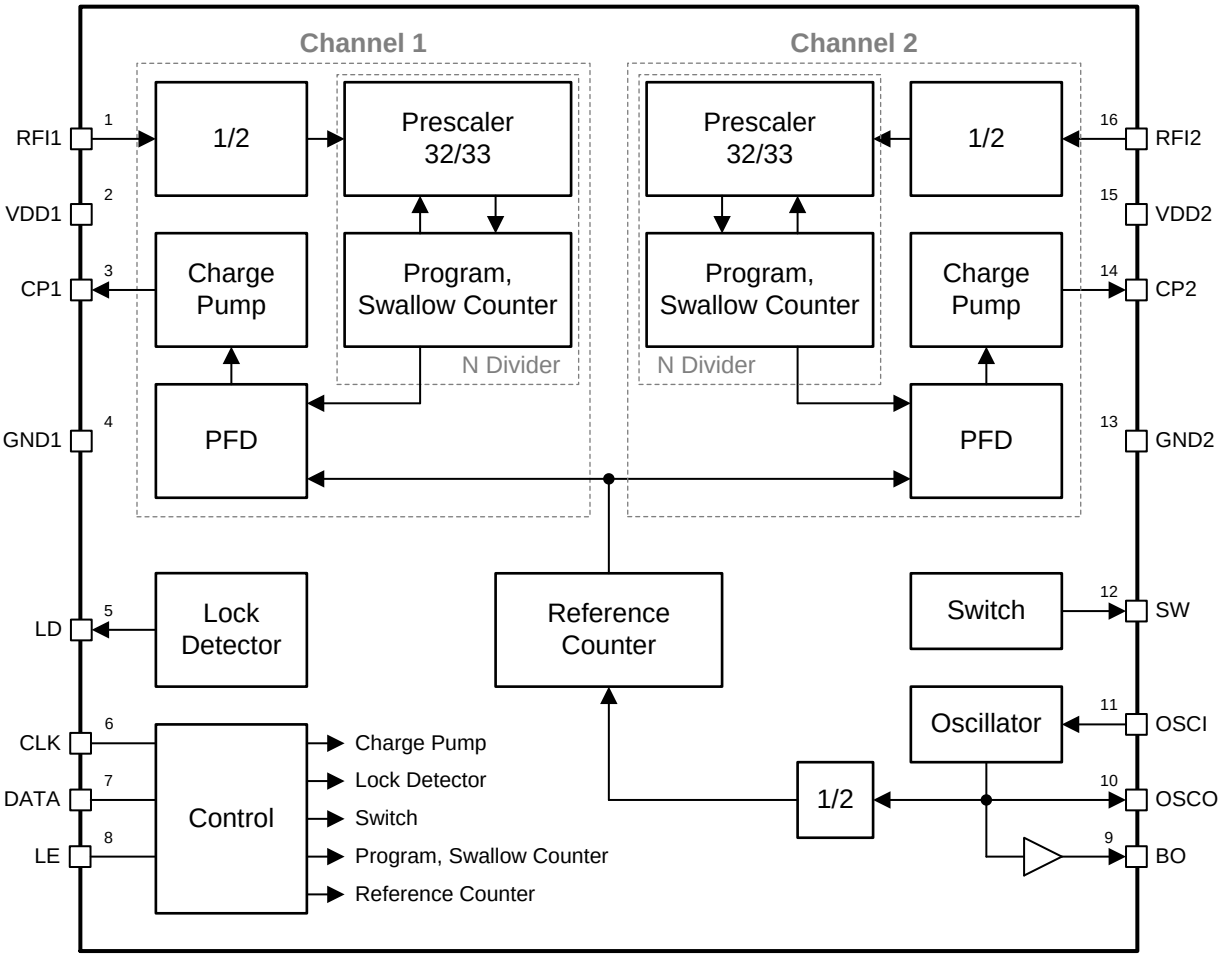
The DHL214D is an integrated dual frequency synthesizer with prescaler. It consists of a dual-modulus prescaler, programmable program(P) and swallow(S) counter, programmable reference(R) counter, a phase frequency detector(PFD) and a charge pump. A PLL can be completely implemented with external loop filter and voltage controlled oscillator(VCO). It is available in a 16-pin TSSOP plastic package.

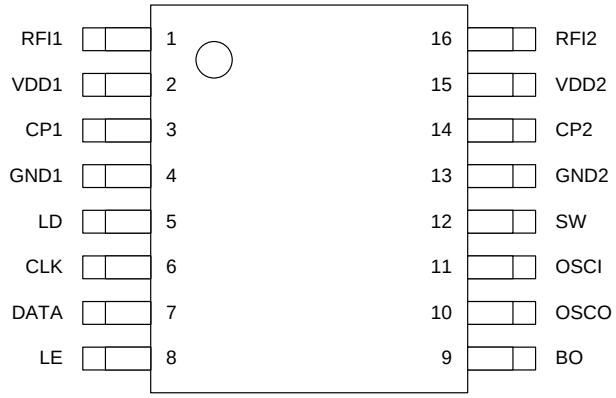
Features

- Two systems for transmitter and receiver
- Wide frequency range (50MHz to 1.4GHz)
- Wide supply voltage range (2.4V ~ 5.5V)
- Selectable charge pump current (0.2mA, 0.4mA, 0.8mA, 1.6mA)
- Selectable power down
- Lock detection
- 3-wire serial interface
- GP214D compatible

Block Diagram and Application Circuit



Pin Description



Pin No.	Mnemonic	I/O	Description
1	RFI1	I	Channel 1 RF input.
2	VDD1	-	Power supply. VDD1 and VDD2 are connected to each other.
3	CP1	O	Channel 1 charge pump output.
4	GND1	-	Ground for Channel 1 PLL, counters, lock detector and control circuit
5	LD	O	Lock detect output or counter output. (NMOS open drain)
6	CLK	I	Serial clock input. (Do not open)
7	DATA	I	Serial data input. (Do not open)
8	EN	I	Serial data load enable. (Do not open)
9	BO	O	Oscillator output's buffered output.
10	OSCO	O	Reference oscillator output.
11	OSCI	I	Reference oscillator input. Typically connect to TCXO
12	SW	O	Switchover terminal for the time constant of loop filter. (NMOS open drain)
13	GND2	I	Ground for Channel 2 PLL, switch, oscillator and common internal bias.
14	CP2	O	Channel 2 charge pump output.
15	VDD2	-	Power supply. VDD1 and VDD2 are connected to each other.
16	RFI2	I	Channel 2 RF input.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Power Supply Voltage		V_{DD}	-0.3 to 6.0	V
Input/Output Voltage		V_{IN}, V_{OUT}	-0.3 to 6.0	V
Operating Temperature Range		T_{OP}	-30 to +85	°C
Storage Temperature Range		T_{ST}	-35 to +125	°C
ESD	HBM (Human Body Model)	V_{HBM}	2000	V
	MM (Machine Model)	V_{MM}	200	V

This device is a high performance RF integrated circuit and is ESD sensitive. Proper precautions should be taken for handling and assembly.

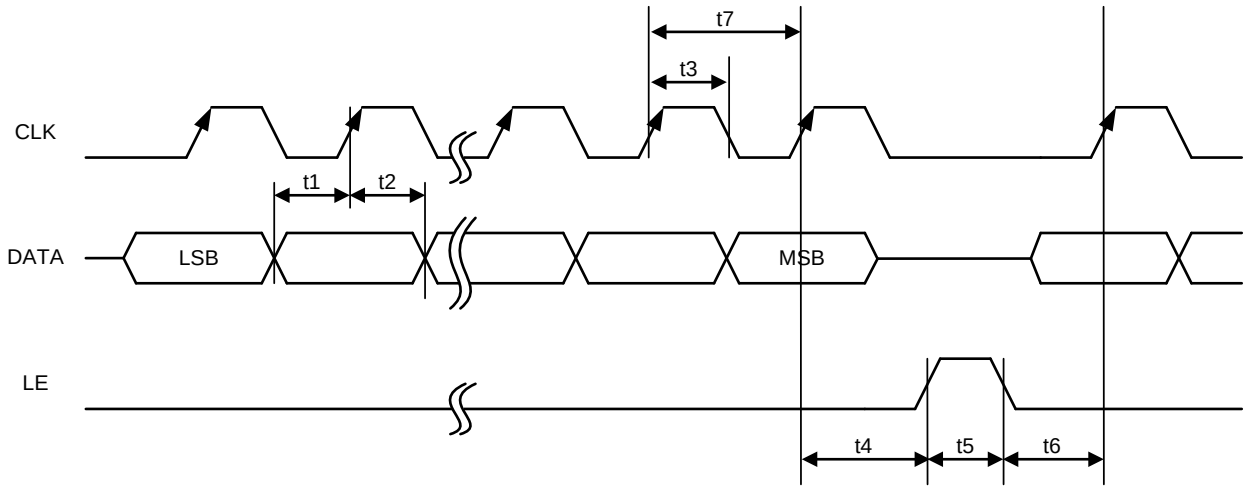
Electrical Characteristics

(V_{DD}=3V, Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}			2.4	3.0	5.5	V
Power Supply Current	I_{DD}	$f_{IN1,2}$ = 675MHz -5dBm f_{OSC} = 20MHz 0dBm	V_{DD}=3V	5	8	11	mA
			V_{DD}=5V	7	10	13	
Standby Current	I_{SB}	standby mode			0.1	10	uA
RFI1,2 Input Operating Frequency	$f_{IN1,2}$	-10dBm		50		1400	MHz
RFI1,2 Input Sensitivity Power	P_{FIN}	50~100MHz	V_{DD}=2.4~3.6V	-10		5	dBm
		100~1000MHz	V_{DD}=2.4~3.6V	-15		5	
			V_{DD}=3.6~5.5V	-10		5	
		1000~1400MHz	V_{DD}=2.4~3.6V	-10		5	
OSCI Input Operating Frequency	f_{OSC}	0dBm		4		40	MHz
OSCI Input Sensitivity Power	P_{OSC}	4 ~ 40MHz		-15		10	dBm
Logic High-Level Input Voltage	V_{IH}			2.0		5.5	V
Logic Low-Level Input Voltage	V_{IL}			-0.3		0.8	V
Logic Input Leakage Current	I_{IH}			-10		10	uA
Logic Low-Level Output Voltage	V_{OL}	I_{OL} = 1mA				0.4	V
CP1, CP2 Output Current	I_{CP1}	CP1=0, CP2=0, V_{CPO}=1.5V			±1.6		mA
	I_{CP2}	CP1=0, CP2=1, V_{CPO}=1.5V			±0.2		mA
	I_{CP3}	CP1=1, CP2=0, V_{CPO}=1.5V			±0.4		mA
	I_{CP4}	CP1=1, CP2=1, V_{CPO}=1.5V			±0.8		mA
CP1, CP2 Cutoff Leakage Current	I_{LEAKCP}	V_{CPO}=0.5V to 4.5V		-1		1	uA

Serial Data Input Timing Characteristics

The serial data is clocked in on the rising edge of clock and transferred into the shift register composed of 17-bit data field and 2-bit control field. When LE is high, stored data is latched. Data is entered LSB first.



Parameter	Minimum Limit	Unit	Description
t1	100	ns	DATA to CLK setup time
t2	200	ns	DATA to CLK hold time
t3	200	ns	CLK pulse width high
t4	100	ns	CLK to LE setup time
t5	200	ns	LE pulse width high
t6	200	ns	LE to CLK setup time
t7	1000	ns	CLK period

Group Code (GC1, GC2)

The data stored in the shift register is loaded into one of four appropriate latches depending on the state of group code(GC1, GC2) listed below.

GC2	GC1	Destination of Serial Data
0	0	Control Latch
1	0	Channel 1 Program Counter(P) and Swallow Counter(S) Latch
0	1	Channel 2 Program Counter(P) and Swallow Counter(S) Latch
1	1	Reference Counter(R) Latch

Control Latch

The control register enables various functions shown in the table below.

LSB													MSB
Test Mode	PFD Polarity	Channel 1			Channel 2			Ref. Counter Standby	Lock Detector		Filter Switch	Group Code	
		Charge Pump Output Current		Standby	Charge Pump Output Current		Standby						
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
T	FC	CP1	CP2	SB1	CP1	CP2	SB2	SBR	LD1	LD2	SW	GC2 “0”	GC1 “0”

T	Test Mode Selection
0	Normal Mode
1	Test Mode

FC	Phase Frequency Detector(PFD) Polarity
0	Positive (When the VCO characteristics are positive)
1	Negative (When the VCO characteristics are negative)

CP1	CP2	Charge Pump Output Current
0	0	±1600μA
0	1	±200μA
1	0	±400μA
1	1	±800μA

LD Output State

The LD output state can be selected via controlling T, SB1, SB2, LD1 and LD2.

T	SB1	SB2	LD1	LD2	LD Output State
0	0	0	0	0	Low
			0	1	Channel2 Lock Detect
			1	0	Channel1 Lock Detect
			1	1	Channel1 Lock Detect and Channel2 Lock Detect
		1	0	0	Low
			0	1	High
			1	0	Channel1 Lock Detect
			1	1	Channel1 Lock Detect
	1	0	0	0	Low
			0	1	Channel2 Lock Detect
			1	0	High
			1	1	Channel2 Lock Detect
		1	0	0	Low
			0	1	High
			1	0	High
			1	1	High
1	1	0	0	0	Low
			0	1	Channel2 Prescaler Output
			1	0	Chennel2 N Divider Output
			1	1	Reference Counter Output
	0	1	0	0	Low
			0	1	Channel1 Prescaler Output
			1	0	Chennel1 N Divider Output
			1	1	Local Oscillator Output divided by 2
	1	1	×	×	Reserved (Do Not Use)
	0	0	×	×	Reserved (Do Not Use)

Programmable Standby Mode (SB1, SB2 and SBR)

Standby mode is controlled by three control bits of SB1, SB2 and SBR. The standby control of channel 1 and channel 2 can be made by SB1 and SB2. The on/off of reference divider (from oscillator to reference counter) is controlled by SBR.

SB1	SB2	SBR	CH1 Status	CH2 Status	Reference Divider Status	Mode
0	0	0	ON	ON	ON	Inter-locking
0	1	0	ON	OFF	ON	CH1 locking
1	0	0	OFF	ON	ON	CH2 locking
1	1	0	OFF	OFF	ON	Reference Divider ON
1	1	1	OFF	OFF	OFF	Standby

Loop Filter Switch Control (SW)

For switching time constant of loop filter, SW pin is controlled by “SW” bit.

SW	Mode
0	High Lock (internal open-drain NMOS ON)
1	Normal Lock (internal open-drain NMOS OFF)

Reference Counter (R)

When the control bits (GC1, GC2) are “11”, data is transferred from shift register into the reference counter latch which sets the divide ratio of 12-bit reference counter. The divide ratio is programmed using the bits as shown in the table below.

LSB													MSB
12-bit Reference Counter												**Group Code**	
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	GC2 “1”	GC1 “1”

12-bit Reference Counter

Divide Ratio	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•••	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Divide ratios less than 3 are prohibited.

Reference divider’s divide ratio (from oscillator input to PFD input) : 2×R = 2×(3 to 4095) = 6 to 8190

Program Counter (P) and Swallow Counter (S), CH1 AND CH2

These counters consist of the 5-bit swallow counter, the 12-bit program counter, and two modulus prescaler providing divisions of 64 and 66. The swallow counter and program counter enable to set any of 192 to 262142 divisions.

LSB																	MSB		
5-bit Swallow Counter					**12-bit Program Counter**												**Group Code**		
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	
S1	S2	S3	S4	S5	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	GC2	GC1	
																	“1”	“0”	CH1
																	“0”	“1”	CH2

12-bit Program Counter (P)

Divide Ratio	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•••	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Divide ratios less than 3 are prohibited.

Divide ratio : 3 to 4095

5-bit Swallow Counter (S)

Divide Ratio	S5	S4	S3	S2	S1
0	0	0	0	0	0
1	0	0	0	0	1
•••	•	•	•	•	•
31	1	1	1	1	1

Divide ratio : 0 to 31, P ≥ S

RF divider’s divide ratio (from RFI to PFD input) = 2 × (32 × P + S), P ≥ S : 192 to 262142

Example

A 21.25MHz crystal oscillator is connected, being divided into 25kHz steps. (Reference frequency is 12.5kHz)

Reference divider’s divide ratio = 2 X R = 21.25MHz / 12.5KHz

R = 850

A Signal of 450 MHz is entered into RFI1, being divided into 25 kHz step. (Reference frequency is 12.5kHz)

RF divider’s divide ratio = 2 × (32 × P + S) = 450MHz / 12.5KHz

P = 562, S = 16

Pulse Swallow Function

$$f_{VCO} = 2 \times (32 \times P + S) \times \{ f_{OSC} / (2 \times R) \} (P \geq S)$$

f_{VCO} : The output frequency of external voltage controlled oscillator(VCO)

P : The preset divide ratio of binary 12-bit program counter(P) (3 to 4,095)

S : The preset divide ratio of binary 5-bit swallow counter(S) (0 to 31)

f_{OSC} : The output frequency of the reference oscillator

R : The preset divide ratio of binary 12-bit reference counter(R) (3 to 4,095)

Lock Detect

LD Pin (Output)	T, SB1, SB2, LD1, LD2	Lock State
L	Lock Detect Set	NOT Detected
H		Detected

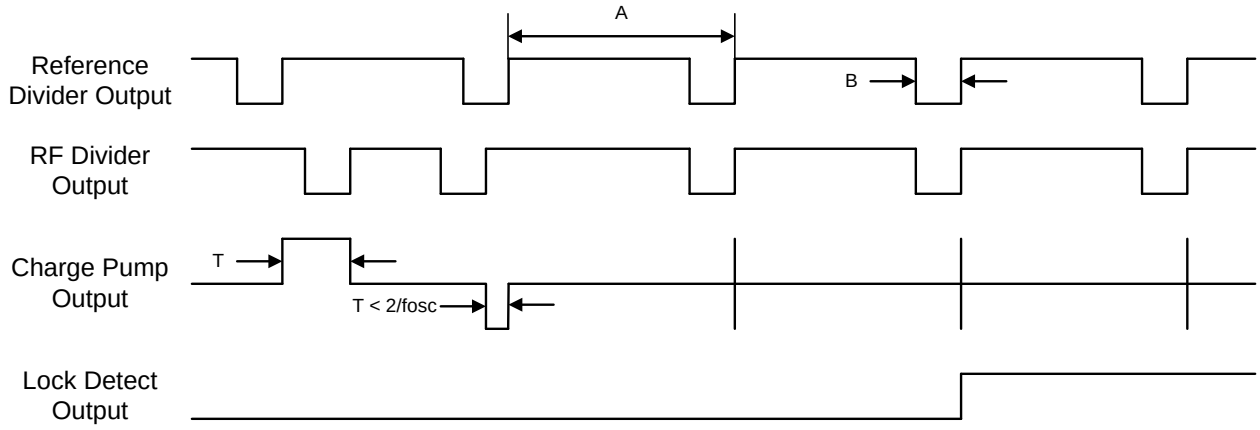
In case where the time difference, “T” less than 2/fosc (T<2/fosc) continues for more than three cycles of reference counter output, LD goes “H”.

fosc : oscillator operating frequency

T : time difference of the pulse between reference divider output and RF divider output

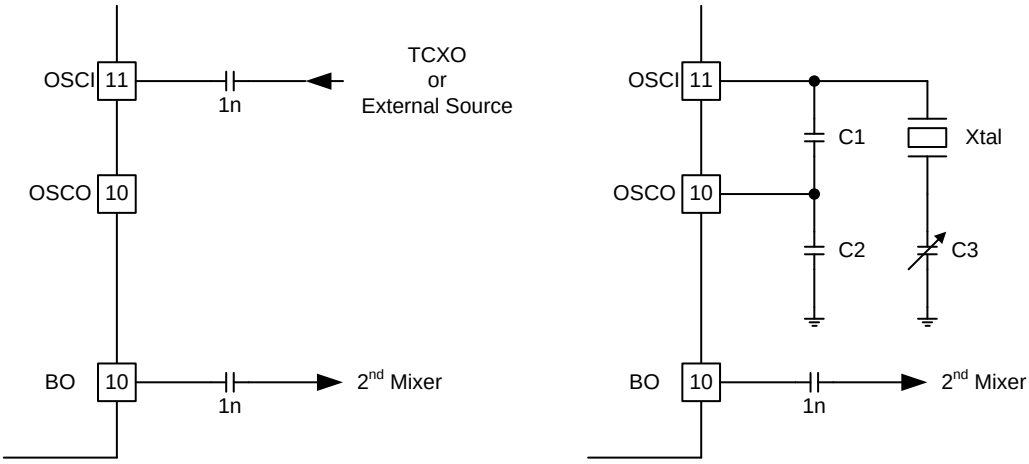
$$A = \frac{\text{Number of divisions by reference dividers}}{\text{fosc}}$$

$$B = \frac{2}{\text{fosc}}$$

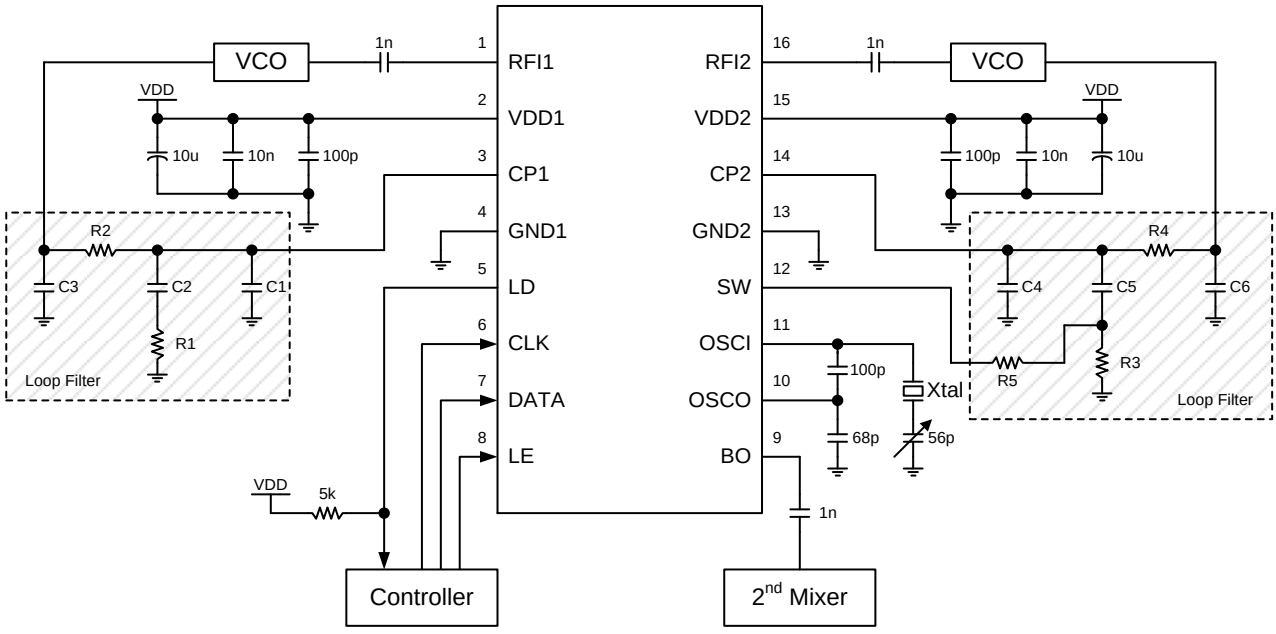


Crystal Oscillator Circuit (OSCI, OSCO) and Buffer Out (BO)

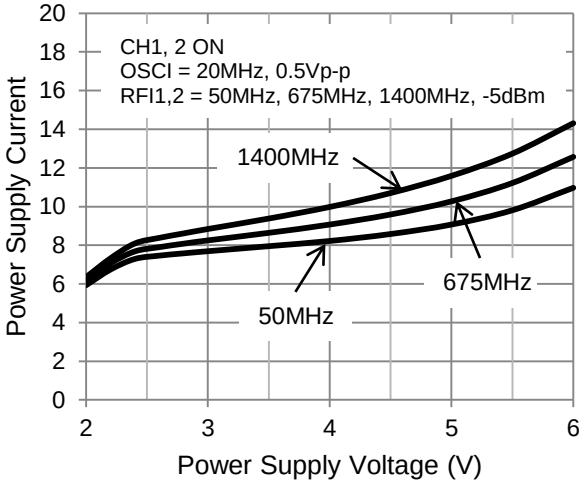
Oscillator can be configured using the crystal or TCXO. The colpitts structure is used for the crystal.

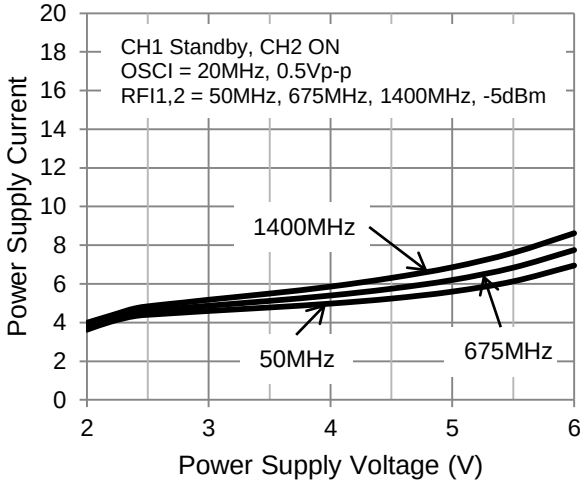


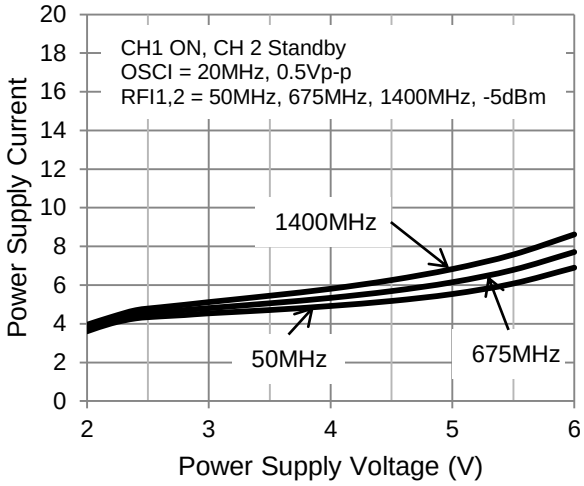
Application Example

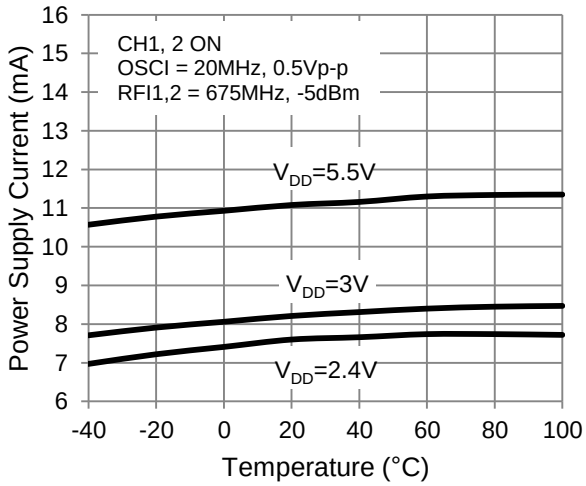


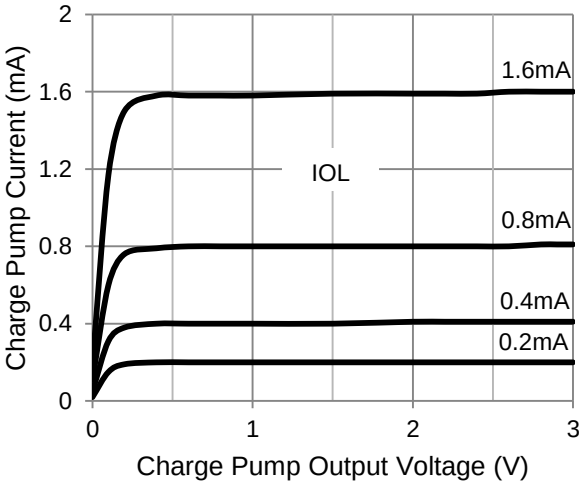
Typical Performance Characteristics

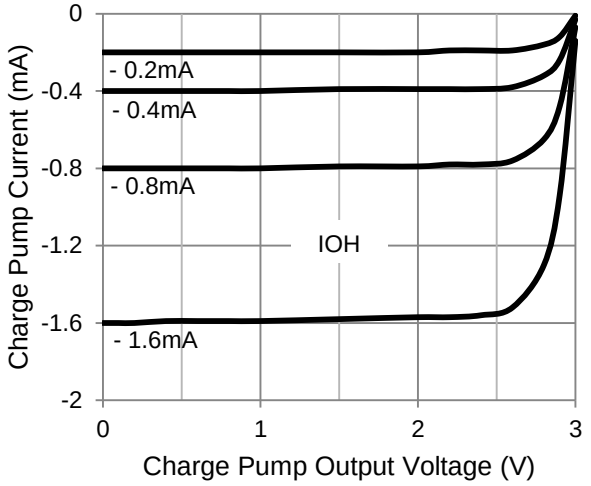


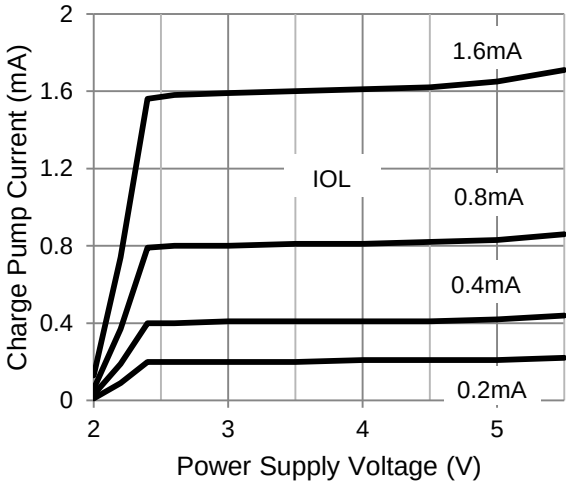


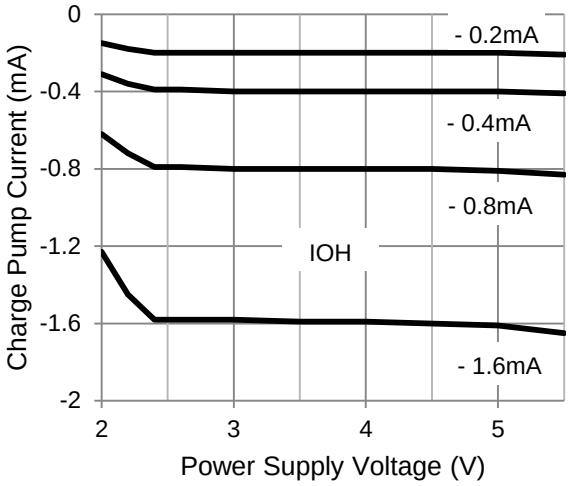


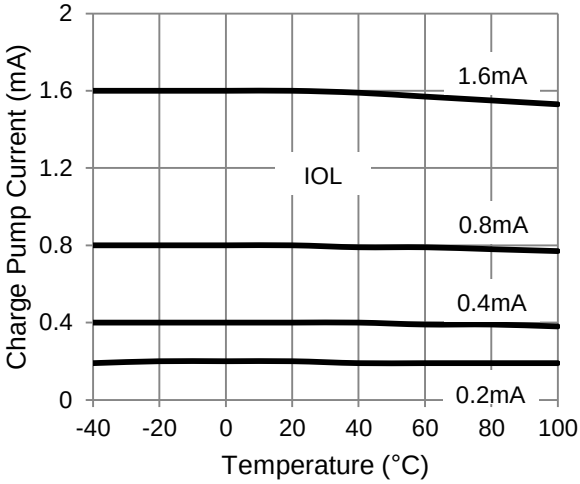


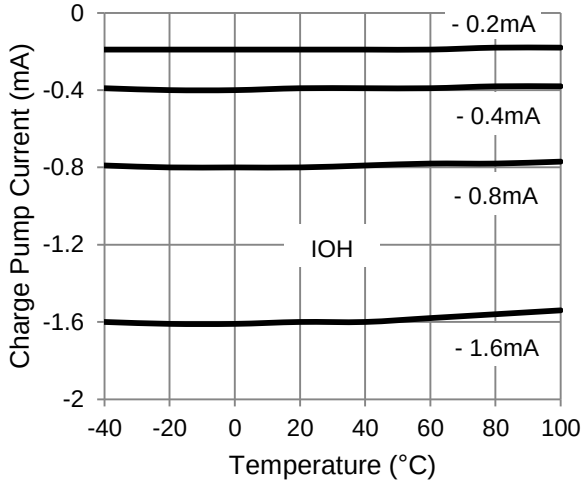












Package Dimensions